Session 17 Overview

Analog Techniques and PLLs

Chair: Vadim Gutnik, *Impinj, Newport Beach, CA*

Associate Chair: Stefan Heinen, *Infineon Technologies, Duisburg, Germany*

Phase-locked loops (PLLs) are ubiquitous and critical blocks in solid-state electronic systems. The stability of clock signals affects the performance and power (and, hence, battery-life) of microprocessors, data converters, radios and cell phones. The first six papers in this session present several PLLs and DLLs that incorporate techniques to overcome various limitations of highly scaled CMOS technologies when used for analog circuits.

The first two papers deal with fractional-N PLLs for wireless applications. Paper 17.1 From UC San Diego demonstrates a 730kHz bandwidth using a 12MHz reference clock, which enables SoC applications such as Bluetooth. The key for achieving the high bandwidth and associated 35µs settling time is an adaptive phase-noise cancellation technique. The next paper, 17.2 from Columbia U, describes a fully integrated 2.5GHz fractional-N PLL in a 90nm CMOS technology operating at 0.65V. The measured performance of this synthesizer complies with Bluetooth requirements.

Using a technique previously limited to data converters, the DLL in Paper 17.3, from Pohang U and Samsung, achieves a wide locking rang of 40 to 800MHz with a very small phase step error of less than 17ps and low jitter ($12ps_{pp}$ and $1.6ps_{rms}$).

In Paper 17.4 from PA Semi, a dual-supply ring-oscillator PLL in 65nm uses a novel ping-pong counter approach and multiple device types to achieve very low jitter (1.5ps) while using only 15mW of power. It has a 50% duty-cycle output and a short critical path, which are both essential for low-noise clock generation. The PLL in Paper 17.5 from Samsung achieves very low power and area via a simple solution; a replica of the oscillator control current is used in the loop filter to ensure that the bandwidth tracks the update rate. Paper 17.6 from IBM shows off a 65nm partially-depleted SOI process with a fast clock generator that has sufficient tuning range to have excellent yield when fabricated.

The next two papers deal with high-speed comparators focusing on low power and low voltage. Paper 17.7 from U Twente describes a high-speed comparator with a large common-mode input range achieved by a folded latch structure. A benchmark for low-voltage and high-speed operation of CMOS comparators is given in Paper 17.8 from TU Vienna. The circuit presented in that paper achieves 600MHz operating speed with a 0.5V supply.

The last paper in the session, Paper 17.9 from Helsinki U and U Turku, shifts the scope to low-power sensor interfaces by demonstrating a 3-axis accelerometer in a 0.13µm CMOS technology.

17.1 A Wide-Bandwidth 2.4GHz ISM-Band Fractional-N PLL with Adaptive Phase-Noise Cancellation **1:30 PM**

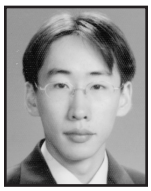
A. Swaminathan, University of California at San Diego, La Jolla, CA

A 2.4GHz ISM-band PLL with a 730kHz bandwidth, a 12MHz reference, an on-chip loop filter, and worst-case phase noise of -101dBc/Hz and -124dBc/Hz at 100kHz and 3MHz offsets, respectively, is enabled by an adaptive phase-noise cancellation technique with 35µs settling time. The 0.18µm CMOS IC measures 2.2×2.2mm^2, and its core circuitry draws 20.9mA from a 1.8V supply.

17.2 A 0.65V 2.5GHz Fractional-N Frequency Synthesizer in 90nm CMOS **2:00 PM**

S-A. Yu, Columbia University, New York, NY

A 2.5GHz fractional-N synthesizer is realized in a digital 90nm CMOS technology. The RF dividers operate at 0.65V while the remainder of the PLL operates at 0.5V; no special devices or voltage boosting is used to achieve the 0.5V operation. The synthesizable range covers 2.4 to 2.6GHz with a phase noise of -55dBc/Hz in band and -120dBc/Hz at a 3MHz offset. The synthesizer dissipates 7mW and occupies 0.14mm^2.



17.3 A 40-to-800MHz Locking Multi-Phase DLL **2:30 PM**

Y-S. Kim, Pohang University of Science and Technology, Pohang, Korea

A delay matrix and a gradual switching of shunt capacitors in delay cells are proposed for a wide-range-locking multi-phase DLL. With an interpolating resistor network, delay step error is greatly reduced by error averaging. The DLL, implemented in 0.13µm CMOS, has a locking range of 40 to 800MHz. With 40 phases, the maximum delay step error is 16.7ps at 700MHz. The chip dissipates 43mW at 700MHz from a 1.2V supply and the measured jitter is 12ps$_{pp}$ and 1.6ps$_{rms}$.

17.4 A Dual-Supply 0.2-to-4GHz PLL Clock Multiplier in a 65nm Dual-Oxide CMOS Process **3:15 PM**

S. Desai, P.A. Semi, Santa Clara, CA

A 0.2-to-4GHz PLL generates the clock for an SoC in a 65nm CMOS process. The PLL uses dual-oxide devices operating in different voltage domains to generate a clock with a wide range of output frequencies and low jitter. The measured rms period jitter is 1.5ps at 2GHz and total power consumed from both the 1.0V and 1.8V supplies is 15mW.

17.5 A 1.2mW 0.02mm^2 2GHz Current-Controlled PLL Based on a Self-Biased Voltage-to-Current Converter **3:45 PM**

W. Jung, Samsung Electronics, Yongin, Korea

A 0.5-to-2GHz frequency synthesizer PLL implemented in a 90nm CMOS technology uses a 1.0V supply and dissipates 0.6 and 1.2mW while operating at 1 and 2GHz, respectively. The PLL occupies an active die area of 0.02mm^2. The current-controlled method based on a self-biased voltage-to-current converter enables the use of a small size loop filter and makes the PLL bandwidth insensitive to PVT variations and multiplication factor.

17.6 A 1V 18GHz Clock Generator in a 65nm PD-SOI Technology **4:00 PM**

F. Gebara, IBM, Austin, TX

Two PLLs were designed using current-steering interpolating ring oscillators. The regular-V_t PLL demonstrates a 3.2× lock range and a maximum frequency of 24.6GHz with 1.28ps$_{rms}$ jitter at 1V. The high-V_t PLL exhibits a 3.5× lock range at 6% lower frequency. The 0.18mm^2 PLLs consume 16mW of power from 1V and are fabricated in a PD-SOI 65nm technology.

17.7 A Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time **4:15 PM**

D. Schinkel, University of Twente, Enschede, The Netherlands

A latch-type voltage sense amplifier in 90nm CMOS is designed with a separated input and cross-coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range. With a 1-σ offset of 8mV, the circuit consumes 92fJ/decision with a 1.2V supply. It has an input equivalent noise of 1.5mV and requires 18ps setup-plus-hold time.

17.8 A 0.12µm CMOS Comparator Requiring 0.5V at 600MHz and 1.5V at 6GHz **4:30 PM**

B. Goll, Vienna University of Technology, Vienna, Austria

This comparator has 2 active-load PMOS transistors that can be used to reset the output nodes to the supply level. An NMOS transistor added in the clock line controls the active loads to avoid additional reset switches and continuously biased load transistors. Two NMOSTs added in the input differential amplifier reduce the power consumption, which is 18µW at 0.5V and 600MHz, and 2.65mW at 1.5V and 6GHz.

17.9 A 62µA Interface ASIC for a Capacitive 3-Axis Micro-Accelerometer **4:45 PM**

M. Paavola, Helsinki University of Technology, Espoo, Finland

An interface ASIC for a capacitive 3-axis micro-accelerometer is implemented in a 0.13µm CMOS process. Die area and power dissipation are reduced by using time-multiplexed sampling and duty cycles down to 0.3%. The chip with 0.51mm^2 active area draws 62µA from a 1.8V supply while sampling 4 proof masses, each at 1kS/s. With a ±4g capacitive 3-axis accelerometer, the measured noise in the x, y and z directions is 460µg/√Hz, 550µg/√Hz and 550µg/√Hz, respectively.